DDR2 1GB FULLY BUFFERED DIMM

P2EFB001G-18RCB6M5I

FEATURES

- JEDEC standard Raw Card B Design
- Industry Standard Advanced Memory Buffer (AMB)
- High-speed differential point-to-point link interface at 1.5V (JEDEC draft spec)
  - -14 north-bound (NB) high speed serial lanes
  - -10 north-bound (SB) high speed serial lanes
- Various features/modes:
  - MBIST and IBIST Test functions
  - Transparent mode and direct access mode for DRAM test support
  - Interface for a thermal sensor and status indicator
- Channel error detection and reporting
- SPD (serial presence detect) with 1 piece of 256 byte serial EEPROM
- Automatic DDR2 DRAM bus and channel calibration

Specifications

- Density: 1GB
- Organization
  ---- 128M words x 72 bits, 2 ranks
- Mounting 18 pieces of 512M bits DDR2 SDRAM sealed in FBGA
- Package
  ---- 240-pin fully buffered, socket type dual in line memory module (FB-DIMM)
  ---- PCB height: 30.35mm
  ---- Lead pitch: 1.00mm
  ---- Advance Memory Buffer (AMB): 655-ball FCBGA
  ---- Lead-free (RoHS compliant)
- Power supply
  ---- DDR2 SDRAM: VDD=1.8V+/- 0.1V
  ---- AMB: VCC=1.5V+0.075V/- 0.045
- Data rate: 667Mbps (Max)
- Four internal banks for concurrent operation (components)
- Interface: SSTL_18
- Burst lengths (BL): 4, 8
- /CAS Latency (CL): 3, 4, 5
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
  ---- Average refresh period
  7.8us at 0°C <TC < +85°C
  3.9us at +85°C <TC < +95°C
- Operating case temperature range
  ---- TC = 0°C to +95 °C

Performance

	FB-DIMM				
System clock Frequency	**Speed grade**	**Peak channel throughput**	**FB-DIMM link data rate**	**Speed Grade**	**DDR data rate**
167MHz	**PC2-5300F**	**8.0GByte/s**	**4.0Gbps**	**DDR2-667 (5-5-5)**	**667Mbps**

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DIMENSIONS, ASSEMBLY DRAWING (TOP and BOTTOM)

Figure 1 shows the placement of all the components on top and bottom layer of 128Mx72 1GB double sided module